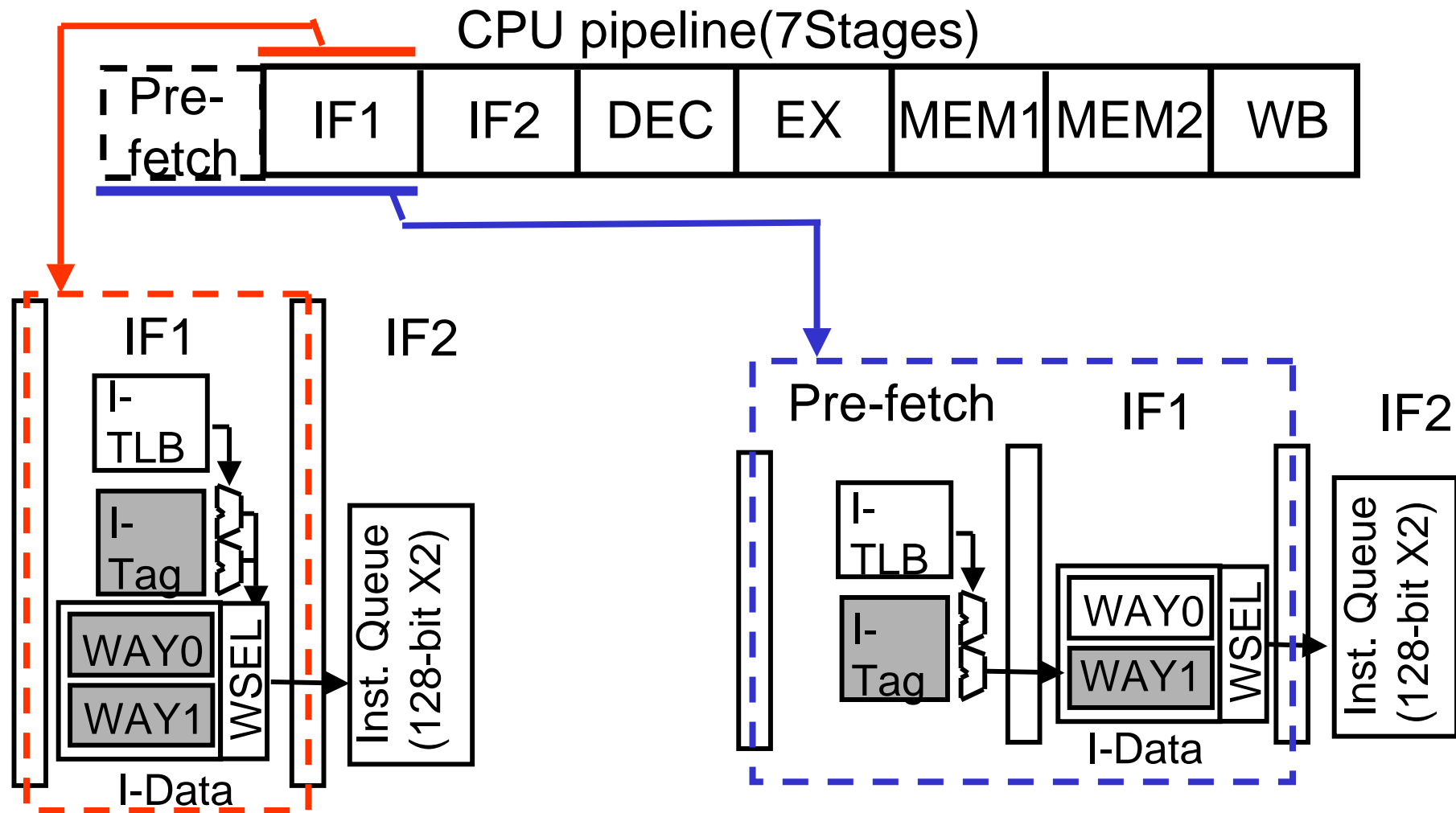


Variable Latency I-Cache



1) Branch Condition

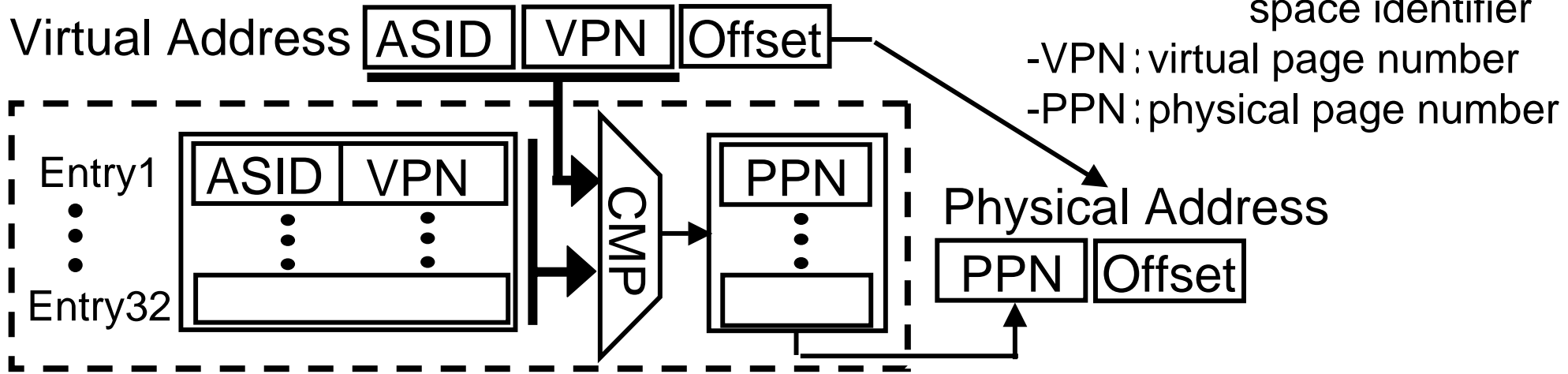
Latency : 1cycle

2) Except for Branch Condition

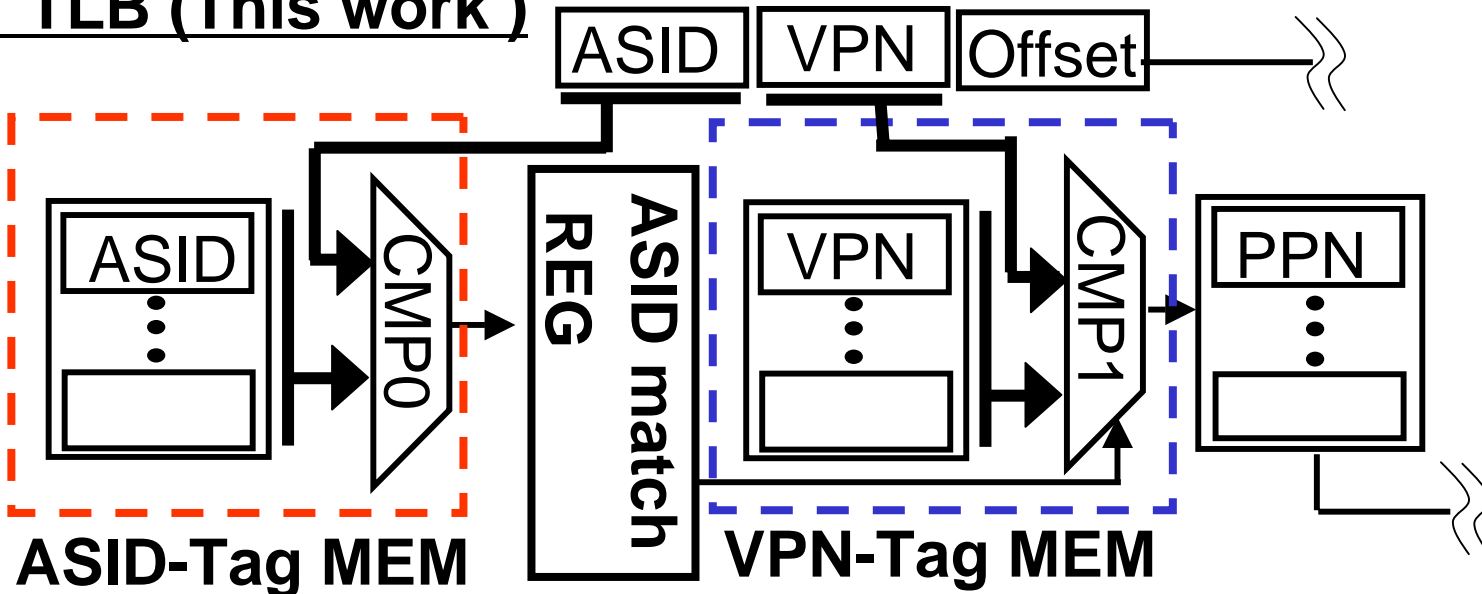
Latency : 2cycles

TLB Design (1/2)

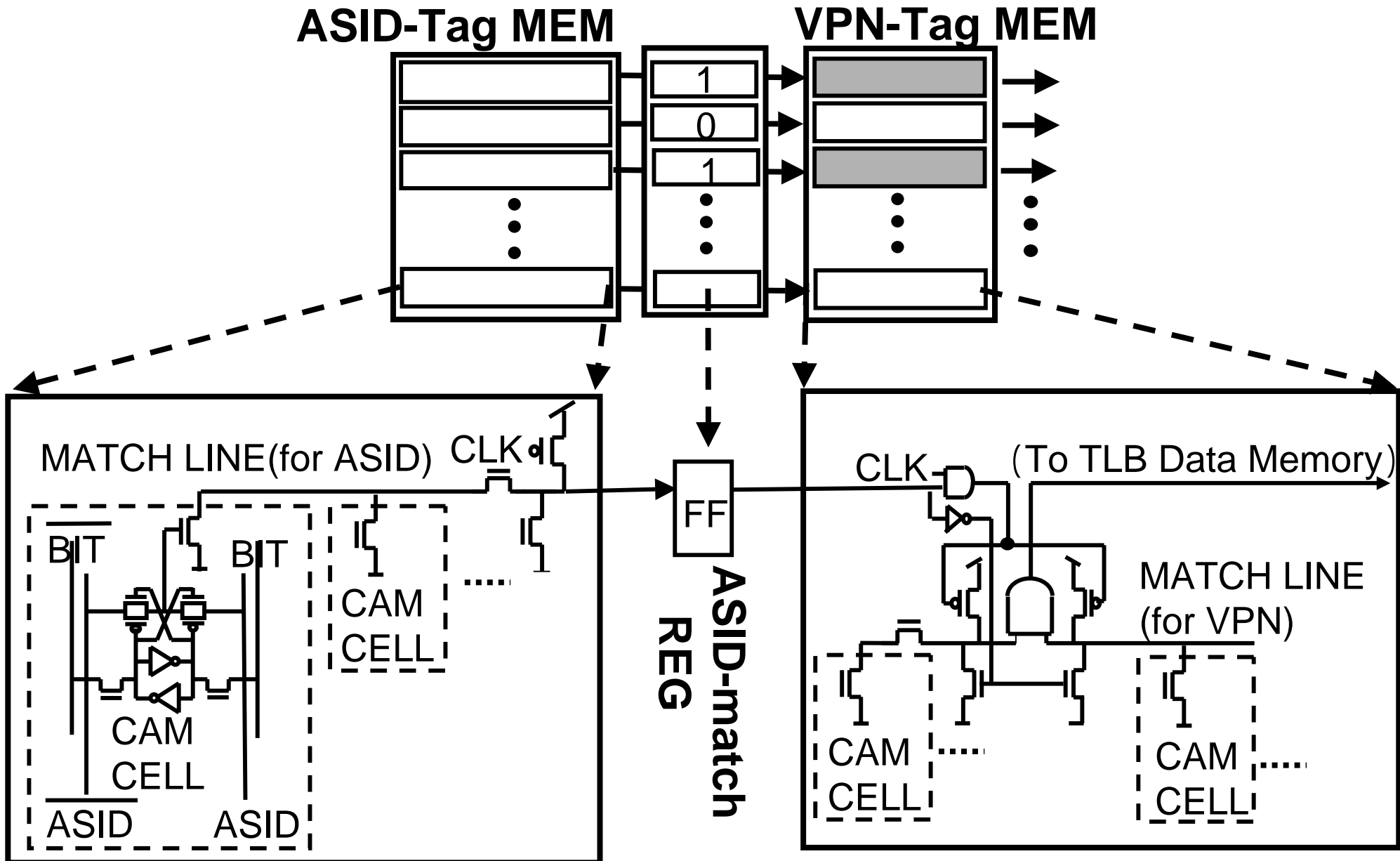
TLB (Conventional)



TLB (This work)



TLB Design (2/2)



Power Consumption(1/2)

Block	Low Power design	Power reduction (Estimation)
CPU Data-path & Ctrl	61% of FF/Latch : Gated controlled	16.3%
Clock	4 Clock Meshes	14.1%
I-Cache	Variable Latency I-Cache	40.0% (All I-Cache Hit)
TLB	Divided into ASID-Tag MEM &VPN-Tag MEM	41.0%

Power Consumption(2/2)

